Full Custom ASIC Design Secrets for Bitcoin and Cryptocurrency Mining

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Abstract

In the competitive world of cryptocurrency mining, power efficiency, hashrate performance, and reliability are paramount. This paper delves into the top-tier full custom ASIC (Application-Specific Integrated Circuit) design, revealing industry secrets and expert methodologies that drive high-performance Bitcoin and cryptocurrency mining. Written by a tech expert from one of the top ASIC miner companies, this paper leverages advanced design techniques, meticulous physical layout, and comprehensive verification processes to showcase the exceptional capabilities of full custom ASICs in maximizing mining efficiency and profitability.

Introduction

The evolution of cryptocurrency mining, particularly Bitcoin mining, has seen a shift from using general-purpose CPUs, FPGAs, and GPUs to specialized ASICs. These ASICs offer unparalleled performance and energy efficiency. Full custom ASIC design represents the pinnacle of this evolution, allowing for tailored solutions that meet the specific demands of mining operations.

Much of the existing literature on ASIC design for cryptocurrency mining comes from academia or non-mining enterprises, which often lacks real-world applicability. To date, only a handful of companies, primarily Chinese (e.g., MicroBT, Bitmain), have successfully developed marketable Bitcoin mining ASICs. This paper seeks to fill that gap by providing insights drawn from actual industry practice, offering a perspective grounded in the realities of the mining sector.

As a professional with over ten years of experience in the tech industry, the author of this paper has developed the world's top Bitcoin ASIC Miner (WhatsMiner), LTC/DOGE and ETH Miners, and played a key role in companies like MicroBT, BTC.COM, and other public fablesses. He has held key

positions in companies listed on NASDAQ, HKSE, and NYSE. With extensive experience in establishing partnerships with TSMC, Texas Instruments, ARM, and Intel, he brings a wealth of knowledge and practical expertise to the field of custom ASIC design for Bitcoin and cryptocurrency mining.

Methodology and Design Flow

Design Philosophy

Our approach to full custom ASIC design is driven by a focus on maximizing PPA (Power, Performance, and Area), particularly under low-voltage operation conditions. This section will describe our design philosophy and methodology:

1. **Pipeline Architecture**: Leveraging the inherent benefits of pipeline structures for mining algorithms, characterized by registers and combinational logic stages. By using a pipeline architecture, we can efficiently handle the high-frequency operations required for cryptocurrency mining.
2. **Manual Netlist and Placement**: Detailed scripting for netlist creation and manual cell placement to optimize critical paths. This allows for precise control over timing and reduces parasitic effects.
3. **Custom Cell Libraries**: Developing specialized cells with optimized transistor counts and dynamic power-saving features. Custom cells are designed to operate at the lowest possible voltages, ensuring minimal power consumption.

Achieving PPA Benefits

Detailed strategies for achieving PPA benefits through custom design:

1. **Custom Register Design**: Utilizing multi-bit registers and latch-based designs to reduce clock power and improve timing borrowing. Multi-bit registers minimize the clock tree's power consumption and reduce overall area.
2. **Manual Placement**: Reducing wire length and balancing setup and hold times to enhance overall performance. Manual placement allows for better control over interconnect delays and crosstalk, improving signal integrity and reducing power consumption.
3. **Optimized Cell Design**: Custom cells are designed to operate at lower voltages, minimizing dynamic power consumption and maximizing efficiency. By tailoring the cell designs to the specific needs of the mining algorithms, we can achieve significant improvements in performance.

Reliability Under Low Voltage

Ensuring the reliability of custom-designed timing logic at low voltages involves:

1. **Accurate Simulation**: Circuit-level simulations to validate custom cell behavior under specific conditions. Tools such as SPICE are used for

detailed electrical simulations to ensure the cells operate correctly under all PVT (Process, Voltage, Temperature) corners.
2. **Consistency in Placement**: Manual placement to ensure uniformity and reduce variability. By controlling the physical layout, we can minimize the impact of process variations and ensure consistent performance.
3. **Precise PVT Calibration**: Verification against process, voltage, and temperature variations. Extensive testing and calibration are performed to ensure the design's robustness across different operating conditions.

Case Studies and Results

Presenting real-world data and case studies from full mask tape-outs:

Project	Process Node	Voltage/Power Efficiency	Algorithm
SC	TSMC 28nm	0.45V, 257J/T	Blake2b
DCR	TSMC 28nm	0.45V, 150J/T	Blake256
DASH	TSMC 16nm	0.38V, 6.2J/G	X11
BTC	TSMC 16nm	0.38V, 65J/T	SHA-256d
BTC	TSMC 7nm	0.30V, 37J/T	SHA-256d
BTC	Samsung 8nm	0.31V, 45J/T	SHA-256d
BTC	SMIC N+1	0.30V, 35J/T	SHA-256d

These results demonstrate the substantial gains in efficiency and performance achievable through our custom design approach.

Integration and Verification

Mixed-Cell Signoff

- **Integration of Custom Cells**: Custom cells are integrated with standard cells from TSMC and other foundries, ensuring compatibility and performance. Custom cells are characterized and validated to match the standard cell library requirements, enabling seamless integration.
- **Signoff Strategies**: Strategies for ensuring seamless compatibility and performance include detailed DRC (Design Rule Check) and LVS (Layout Versus Schematic) checks, as well as timing and power analysis using industry-standard EDA (Electronic Design Automation) tools.

Digital and Analog Co-Design

- **Techniques for Integration**: Integrating digital and analog components to optimize overall chip performance. Techniques such as mixed-signal verification and co-simulation are used to ensure proper integration and functionality.

- **Verification Methodologies**: Methodologies to ensure robustness across different operational conditions include corner analysis, Monte Carlo simulations, and reliability verification to address aging and electromigration.

Conclusion

Full custom ASIC design offers significant advantages for Bitcoin and cryptocurrency mining, providing unparalleled performance, power efficiency, and reliability. By unveiling the secrets of top-tier custom ASIC design, this paper highlights the methodologies and innovations that set industry leaders apart. As cryptocurrency mining continues to evolve, custom ASICs will play a crucial role in driving the next generation of high-efficiency, high-performance mining hardware.